REMARKS

Claims 1 to 3, 5 to 12 and 15 to 23 are pending.

The courtesies extended by Examiner File during discussions with applicant's attorney on December 6, 2006, are gratefully appreciated. As pointed out by the undersigned, in light of the very informative advisory action of November 29, 2006, applicant had hoped that a follow-up amendment to the claims, based upon the suggestion in paragraph 4, on pages 3 of the advisory action, would place the application in condition for allowance. Unfortunately, applicant was advised that such amendments would not be entertained at the preset time. As a consequence, applicant has filed a Request For Continued Examination (RCE) which accompanies the present amendment. The amendment itself more concisely defines the invention by specifying that the digital signal is sampled with only a single clock signal - in particular, the reference clock signal - in an effort to conform with the tenor of the comments in item 4, on page 3 of the advisory action of November 29, 2006. It is respectfully submitted that such amendment makes the claims allowable over the art of record.

More particularly, as has been discussed previously, the system disclosed in the Hamre reference uses multiple (two) clock signals, i.e. a nominal clock and an early clock, both of which are derived from the data signal and would still contain some jitter, which may not matter since the results of the early clock are compared to those of the nominal clock. As a result, only a positive jitter peak can be established based

on a statistical error rate performance of the early clock relative to the nominal clock.

The present invention eliminates the need for both the nominal and early clock signals by counting the number of pulses from **only** a single "offset", "jitter-free" reference clock signal that fall in each bit of the digital signal, and comparing that count to a predetermined number that would occur if there was no jitter. Then the number of times, when the number of sampling times in any bit of the digital signal is different from the predetermined number, is counted, and from this count the jitter is determined.

The clock signal according to the present invention is "offset" from the data signal, not just another clock signal, i.e. the delayed clock signal, as in the Hamre reference. In the present invention, the combination of offsetting and making the reference clock signal jitter free enable a single clock signal to provide: *occasions when the number of sampling times in any bit of said digital signal is different from the predetermined number,* whereby the number of occasions derived from the single reference clock signal are used to provide both low and high frequency jitter measurements.

The present invention is much simpler than the device disclosed in the Hamre reference, i.e. does not require the hardware to generate both the nominal and early clock signals, and enables the recovery of both a positive and negative peak by looking for any errors, not just statistical error rate information.

The device disclosed in the Kanack et al reference is designed to **reduce** jitter in an input signal by comparing a first clock signal, which is phase matched to the input signal, to a second "reduced jitter output clock", which naturally has reduced jitter, since it is independently generated by the VCO 48. The first clock signal disclosed in Kanack et al, i.e. the data sampling clock 66, ***"is used to adjust the frequency of VCO 48 allowing locking of VCO 48 to the frequency and phase of incoming input data signal 64."*** (col 4, lines 30 to 32). Accordingly, the first clock signal, which is based on, but not generated from, the input signal is not jitter free. The second clock signal, which is generated by the VCO 48 and the digital filter 42 is the "reduced jitter output clock". The results of the comparison are used to reduce the jitter in the original input signal. Accordingly, Kanack et al do not disclose or even infer generating a jitter free clock signal **from** the input data signal, and then using that jitter free clock signal to **measure** the jitter in the input data signal. As in the Hamre reference, Kanack et al require a pair of clock signals, as well as an independent clock generator to directly reduce the jitter in the input signal, not to measure the jitter using a jitter free clock signal generated from the original data signal.

Furthermore, there is no motivation to take the "reduced jitter output clock" from the Kanack et al reference and compare it to one of the clock signals or even the data signal in the Hamre et al reference, as both disclosures rely on a comparison of two clock signals, while the present invention totally eliminates the need for a second clock signal. Neither reference discloses or even infers the desire or the ability to eliminate one of the clock signals and the required

signal generator by counting when the number of sampling times in any bit of the digital signal is different from a predetermined number. Accordingly, Applicant respectfully disagrees that the combination of two references, each disclosing the use of two independently generated clock signals, will result in the present invention, which requires only a signal self-generated clock signal.

As such, it is respectfully submitted that all of the claims remaining in the application are in condition for allowance. Early and favorable consideration would be appreciated.

Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please charge any shortage in fees due in connection with the filing of this paper, including Extension of Time fees, to Deposit Account No. 50-1465 and please credit any excess fees to such deposit account.

Respectfully submitted,

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